Low Voltage CMOS/CCD Circuitry for Mixed Signal Applications

Sang Hoon Hong and Woodward Yang

Division of Applied Sciences, Harvard University

Cambridge, MA

Abstract

Analog charge domain operations can be effectively performed at low voltage by integrated CMOS/CCD circuitry. Using a standard 2μm CMOS/CCD process from MOSIS, a 32 tap, programmable, analog FIR filter was implemented on a 2.2mm × 2.2mm die (see Figure 3). The circuitry uses standard 5V clock signals and power supplies, can operate up to 10MHz, dissipates approximately 50mW, and has an SNR of 87dB. These techniques can also be extended to lower operating voltages.

1 Introduction

CCD structures are well suited for analog charge operations and can be used in conjunction with CMOS circuitry to implement a wide variety of mixed signal processing tasks. However, high voltages and complex CCD clocking schemes have been a barrier to their incorporation with more common CMOS circuitry. Using a standard 2μm, double poly, double metal CMOS/CCD technology available through MOSIS, we have integrated several mixed-signal CMOS and CCD components to implement a 32 tap, programmable, analog finite impulse response (FIR) filter which operates on standard 5V clock signals and with a single +5V power supply. The entire chip with 32 CCD MDACs, analog CCD delay lines, 128 bits of on-chip CMOS SRAM storage, and a new low voltage CCD output circuit with correlated double sampling was implemented on a 2.2mm × 2.2mm die. A dual-input CMOS integrator and four-phase CCD clocking were utilized to realize low voltage CCD operation. For comparison, typical CCD components and clocking schemes in this type of process technology would require up to 10V clocking signals with substrate bias and output circuitry operating at 12V while typical CMOS switch capacitor implementations would require much larger area and power.

2 Architecture

A simplified schematic of the programmable FIR filter is shown in Figure 1. The 4-bit filter weights are stored on-chip using CMOS SRAM. The analog input voltage, Vin and stored filter weights are used by the CCD MDACs to generate analog charge packets. These analog charge

This work was supported in part by an NSF Young Investigator Award (MIP-92-57964), an ARO Young Investigator Award (DAAL03-92-G-0375), a grant from Joint Services Electronics Program (N00014-89-J-1023), and by Hamamatsu Photonics.

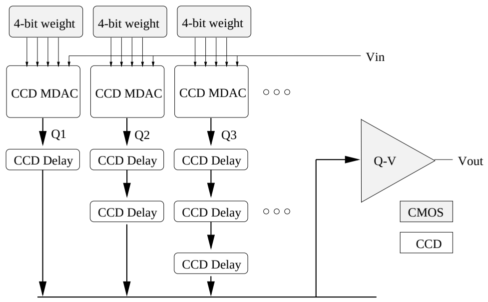

Figure 1: Simplified architecture of the chip.

packets are appropriately delayed through CCD shift registers arranged in a pipeorgan architecture [1] to realize a 32 tap FIR filter. The analog charge packets from the CCD shift registers are summed and converted into an analog output voltage through the CMOS integrator. While the transposed FIR filter requires larger active area than a direct implementation with a single analog CCD delay line, the pipeorgan architecture is more robust for CCD implementation since there is no need for multiple, matched Q-V converters and long term analog voltage storage.

3 CCD Structures

Unit-sized dual-gate CCD input structures were used to implement CCD MDACs [2]. By pulsing an input diode, an analog charge packet that is proportional to an analog input voltage (Vin - Vref) can be generated and stored by a pair of CCD gates. In the past, the dual-gate CCD input structure was enabled/disabled by utilizing an extra control gate to isolate the input structure from the pulsed input diode. However, a more efficient CCD input structure was implemented by conditionally clocking each individual input diode. Thus, the extra CCD control gate can be eliminated by connecting the filter weights through a NAND gate to the CCD MDAC input diode.

The analog delay lines were implemented using buried channel CCDs for high transfer efficiency. Although many CCD components utilize two-phase or uniphase clocking schemes which tradeoff simple clock phase generation for higher clock voltages, four-phase CCD clocking was found to be essential for low voltage 5V clock signals. In the future, on-chip four phase CMOS clock generation circuitry can be integrated.

4 CMOS Output Buffer

The output signal charge from a CCD is typically transferred onto a floating diffusion, and the resulting change in voltage is sensed through a simple NMOS source-follower buffer. However, this simple NMOS circuitry requires a high voltage reset signal to reset the floating diffusion and suffers from both clock coupling to the output sense node, kTC noise, and nonlinear capacitance components. Low voltage operation of this simple circuitry increases the nonlinear capacitance component and significantly reduces the output signal voltage range due to both the inability to pull charge out of the CCD and the voltage drop through the NMOS source-follower. To facilitate operation at low voltage, we have implemented an active CMOS integrator as shown in Figure 2 which only requires 5v power supply. The CMOS integrator utilizes a dual-input structure [3] to precharge the integration capacitor and maximize the output voltage signal range. In addition, the CCD floating node is pinned to a high voltage to insure complete charge transfer out of the buried channel CCD. Operation of the dual input CMOS integrator starts by closing both switches and precharging the integrating capacitor to approximately 4V. Charge injection from the NMOS switch is effectively reduced by using a large holding capacitor on VINN2. When the electrons are clocked out of the CCD, the signal charge is transferred to a programmable integrating capacitor and the output voltage will increase from the initial reset voltage of 1V up to 4V, the opamp output saturation voltage. The circuitry of the dual input

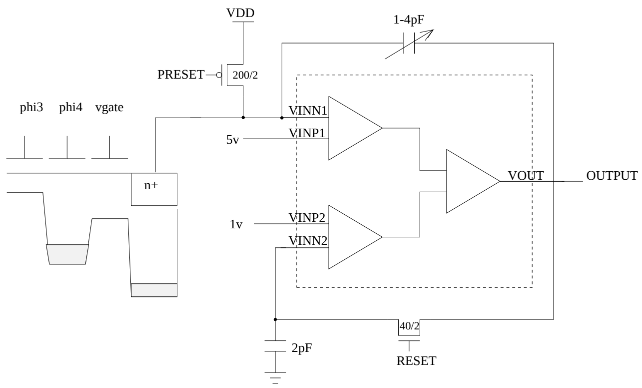

Figure 2: Output circuitry.

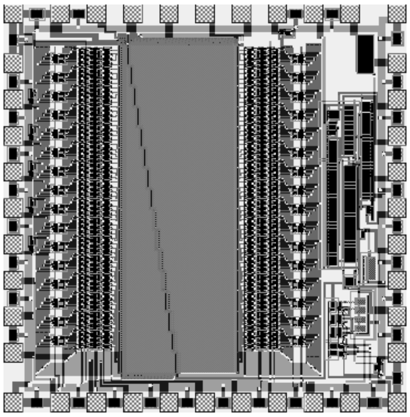

Figure 3: The programmable chip

CMOS opamp is implemented using a standard folded cascode architecture with an additional PMOS differential pair. Since the common DC input voltages of VINN1 and VINP1 were relatively high voltages, these were implemented using NMOS differential pair to extend the input range toward higher voltages. VINN2 and VINP2 were similarly implemented as PMOS differential pair to extend their input range toward to lower voltages. The integrating capacitor can be further programmed through two select lines between a range of 1pF to 4pF.

5 Results and Performance

Figure 4 shows the analog output voltage step response of the FIR filter for a simple averaging filter with equal tap weights. Another example of functionality is demonstrated in Figure

5. Two signals at 20kHz and 56.25kHz are summed and input into the CMOS/CCD programmable FIR filter. By selecting coefficients properly for a LPF with a 31.25kHz cutoff and approximately 40dB attenuation in the stopband, the higher frequency signal is removed and the resulting output spectrum obtained. The programmable FIR chip can operate at up to 10MHz, dissipates approximately 50mW, and has a SNR of 87dB.

6 Conclusion

A 32 tap, programmable analog FIR filter was implemented using low voltage CMOS/CCD components. CCD structures were used as MDACs and staggered delay lines in a pipeorgan architecture. A new CMOS output circuit for low voltage (5V) CCD operation and low voltage (5V) four-phase CCD clocking were demonstrated. This FIR filter chip can also be used as a building block to implement both two- and four-quadrant multiplication, to realize larger analog FIR and IIR filters, and for various adaptive signal processing applications. The integration of CCD structures with CMOS circuitry enables the implementation of compact, low voltage, analog charge domain signal processing. These CMOS/CCD circuits can be extended for use at lower voltages and can also be used to implement a variety of other mixed-signal processing functions. The speed of this CMOS/CCD implementation is limited by the CMOS circuitry since the CCD structures are intrinsically able to operate at hundreds of MHz.

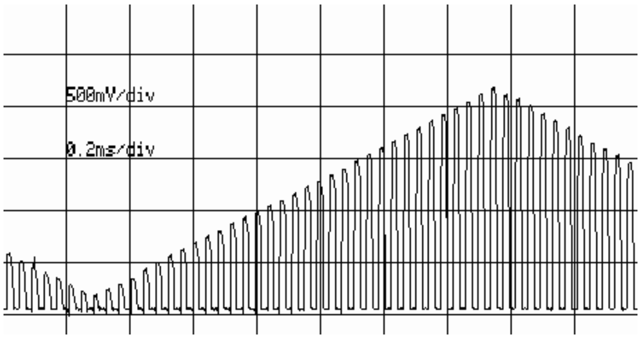

Figure 4: Sample step response for a full scale averaging filter.

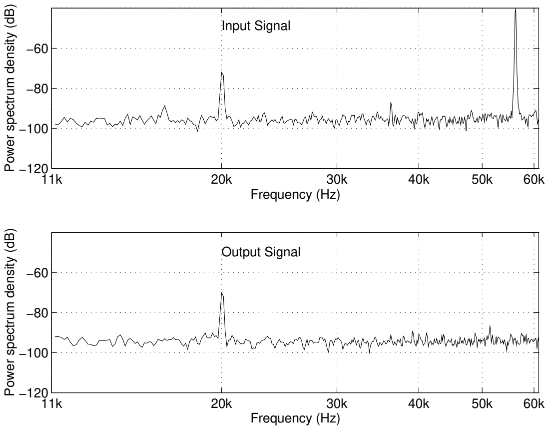

Figure 5: Functioning as LPF

References

[1] A.M. Chiang and B.E. Burke, "A High Speed CCD Digitally Programmable Transversal Filter," *IEEE Journal of Solid-State Circuits*, pp.745-753, vol.SC-18, no.6, 1983.

[2] A.M. Chiang, "A CCD Programmable Signal Processor," *IEEE Journal of Solid-State Circuits*, pp.1510-1517, vol.25, no.6, 1990.

[3] E. Sackinger and W. Guggenbuhl, "A Versatile Building Block: The CMOS Differential Difference Amplifier," *IEEE Journal of Solid-State Circuits*, vol.SC-22, pp.287-294, 1987.